(1390 REV. 5-93) US DEPT. OF COMMERCE PATENT & TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER
107281

U.S. APPLICATION NO.
(if known, see 37 C.F.R.1.5)
09/673208

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INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/00894	February 17, 2000	February 18, 1999

TITLE OF INVENTION
SEMICONDUCTOR DEVICE, MOUNTING SUBSTRATE AND METHOD OF MANUFACTURING MOUNTING SUBSTRATE, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

APPLICANT FOR DO/EO/US
Nobuaki HASHIMOTO

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.

2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.

3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).

4. ☐ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.

5. ☒ A copy of the International Application as filed (35 U.S.C. 371(c)(2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)

6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).

7. ☐ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☐ have not been made and will not be made.

8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).

9. ☒ An oath or declaration of the inventor (35 U.S.C. 371(c)(4)).

10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.

12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.

13. ☒ A FIRST preliminary amendment.

    ☐ A SECOND or SUBSEQUENT preliminary amendment.

14. ☐ A substitute specification.

15. ☐ Entitlement to small entity status is hereby asserted.

16. ☒ Other items or information: PCT Request

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
09/673208	PCT/JP00/00894	107281

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
Basic National fee (37 CFR 1.492(a)(1)-(5)):		
Search Report has been prepared by the EPO or JPO $860.00		
International preliminary examination fee paid to USPTO (37 CFR1.482) $690.00		
No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2)) $710.00		
Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO.....$1,000.00		
International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4).....$ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	53- 20 =	33	X $ 18.00	$594.00	
Independent Claims	13- 3 =	10	X $ 80.00	$800.00	
Multiple dependent claim(s)(if applicable)			+ $270.00	$	
TOTAL OF ABOVE CALCULATIONS =				$2,254.00	
Reduction by 1/2 for filing by small entity, if applicable.			-	$	
SUBTOTAL =				$2,254.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 month from the earliest claimed priority date (37 CFR 1.492(f)).			+	$	
TOTAL NATIONAL FEE =				$2,254.00	
				Amount to be refunded	$
				Charged	$

a. ☒ Check No. 112748 in the amount of $2,254.00 to cover the above fees is enclosed.
b. ☐ Please charge my Deposit Account No. _____ in the amount of $_____ to cover the above fees. A duplicate copy of this sheet is enclosed.
c. ☒ The Director is hereby authorized to charge any additional fees which may be required, or credit any overpayment, to Deposit Account No. 15-0461. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

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(1390 Rev.10-00)

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of

Nobuaki HASHIMOTO

Application No.: New U.S. National Stage of PCT/JP00/00894

Filed: October 13, 2000 Docket No.: 107281

For: SEMICONDUCTOR DEVICE, MOUNTING SUBSTRATE AND METHOD OF MANUFACTURING MOUNTING SUBSTRATE, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

PRELIMINARY AMENDMENT

Director of the U.S. Patent and Trademark Office
Washington, D. C. 20231

Sir:

Prior to initial examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend claims 22-27 as follows:

Claim 22, line 2, change "any of claims 1, 4, 7, and 10." to -- claim 1. --.

Claim 23, line 2, change "any of claims 2, 5, 8, and 11." to -- claim 2. --.

Claim 24, line 2, change "any of claims 3, 6, 9, and 12." to -- claim 3. --.

Claim 25, line 2, change "any of claims 1, 4, 7, and 10." to -- claim 1. --.

Claim 26, line 2, change "any of claims 2, 5, 8, and 11." to -- claim 2. --.

Claim 27, line, 2, change "any of claims 3, 6, 9, and 12." to -- claim 3. --.

REMARKS

Claims 1-53 are pending. By this Preliminary Amendment, claims 22-27 are amended to eliminate multiple dependent claims. Prompt and favorable examination on the merits is solicited.

Respectfully submitted,

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Date: October 13, 2000

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SEMICONDUCTOR DEVICE, MOUNTING SUBSTRATE AND METHOD OF MANUFACTURING MOUNTING SUBSTRATE, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

TECHNICAL FIELD

The present invention relates to a semiconductor device, a mounting substrate and method of manufacturing the mounting substrate, a circuit board, and an electronic instrument.

BACKGROUND ART

Semiconductor devices such as T-CSP (Tape-Chip Scale/Size Package) are known, which use a substrate on which an interconnect pattern is formed. Commonly, a semiconductor chip is mounted on the substrate, and with the electrodes of the semiconductor chip electrically connected to the interconnect pattern, solder balls are provided. The characteristics required of the surface of the interconnect pattern for connecting the electrodes of the semiconductor chip and the characteristics required for providing the solder balls are different. Although the surface of the interconnect pattern requires locally varying characteristics, conventionally the whole of the surface of the interconnect pattern has been subjected to a single plating operation.

DISCLOSURE OF THE INVENTION

The present invention solves the above described problem, and has as its objective the provision of a semiconductor device

including an interconnect pattern having portions of its surface with different properties, and similarly a mounting substrate and method of manufacture thereof, a circuit board, and an electronic instrument.

(1) A semiconductor device of the present invention comprises:

a substrate in which a plurality of through holes are formed;

an interconnect pattern formed on the substrate and passing over the through holes;

a first plating layer formed on the interconnect pattern surface opposite to the substrate;

a second plating layer formed on the interconnect pattern surface looking toward the substrate in the through holes;

a semiconductor chip mounted on the substrate and electrically connected to the first plating layer;

a resin provided on the first plating layer; and

a conductive material provided on the second plating layer,

wherein the first and second plating layers have different properties.

According to the present invention, since the first and second plating layers are formed on the interconnect pattern, oxidation of the surface of the interconnect pattern can be prevented, and also the electrical contact resistance can be lowered.

The first and second plating layers have different

characteristics. A plating layer having appropriate adhesion properties with a resin and a plating layer having appropriate adhesion with a conductive material commonly require different properties. The present invention provides for this by means of the first and second plating layers of different properties.

(2) A semiconductor device of the present invention comprises:

a substrate;

a first interconnect pattern formed on one surface of the substrate;

a second interconnect pattern formed on the other surface of the substrate and electrically connected to the first interconnect pattern;

a first plating layer formed on the first interconnect pattern surface opposite to the substrate;

a second plating layer formed on the second interconnect pattern surface opposite to the substrate;

a semiconductor chip mounted on the substrate and electrically connected to the first plating layer;

a resin provided on the first plating layer; and

a conductive material provided on the second plating layer,

wherein the first and second plating layers have different properties.

According to the present invention, since the first and second plating layers are formed on the first and second interconnect patterns, oxidation of the surface of the first

and second interconnect patterns can be prevented, and also electrical contact resistance can be lowered. The first and second plating layers have different characteristics. A plating layer having appropriate adhesion properties with a resin and a plating layer having appropriate adhesion with a conductive material commonly require different properties. The present invention provides for this by means of the first and second plating layers of different properties.

(3) A semiconductor device of the present invention comprises:

a substrate;

an interconnect pattern formed on the substrate;

a first plating layer formed on a first portion of the interconnect pattern surface opposite to the substrate;

a second plating layer formed on a second portion of the interconnect pattern surface opposite to the substrate;

a resin provided on the first plating layer;

a conductive material provided on the second plating layer; and

a semiconductor chip mounted on the substrate and electrically connected to the conductive material,

wherein the first and second plating layers have different properties.

According to the present invention, since the first and second plating layers are formed on the interconnect pattern, oxidation of the surface of the interconnect pattern can be prevented, and the electrical contact resistance can be lowered.

The first and second plating layers have different characteristics. A plating layer having appropriate adhesion properties with a resin, and a plating layer having appropriate adhesion with a conductive material commonly require different properties. The present invention provides for this by means of the first and second plating layers of different properties.

(4) In this semiconductor device, the first plating layer may be formed to be thinner than the second plating layer.

By making the plating layer thinner, the adhesion properties with the resin are improved, and if the plating layer is made thicker, excellent bonding with the conductive material is obtained.

(5) In this semiconductor device, the first and second plating layers may be formed of different materials.

The first plating layer can be formed of a material improving the adhesion properties with a resin, and the second plating layer can be formed of a material having excellent bonding with the conductive material.

(6) In this semiconductor device, the resin may be an adhesive, and include conductive particles to constitute an anisotropic conductive material; and the semiconductor chip may be mounted by face-down bonding with the anisotropic conductive material interposed.

According to this, an anisotropic conductive material is provided on the first plating layer, and the first plating layer has appropriate adhesion properties with the adhesive of the anisotropic conductive material. By the formation of the first

plating layer, in the face-down bonding of the semiconductor chip, the electrical contact resistance is lowered.

(7) A mounting substrate of the present invention comprises:

a substrate in which a plurality of through holes are formed;

an interconnect pattern formed on the substrate and passing over the through holes;

a first plating layer formed on the interconnect pattern surface opposite to the substrate; and

a second plating layer formed on the interconnect pattern surface looking toward the substrate in the through holes,

wherein the first and second plating layers have different properties.

According to the present invention, since the first and second plating layers are formed on the interconnect pattern, oxidation of the surface of the interconnect pattern can be prevented, and also the electrical contact resistance can be lowered. The first and second plating layers have different characteristics. A plating layer having appropriate adhesion properties with a resin, and a plating layer having appropriate adhesion with a conductive material commonly require different properties. The present invention provides for this by means of the first and second plating layers of different properties.

(8) A mounting substrate of the present invention comprises:

a substrate;

a first interconnect pattern formed on one surface of the substrate;

a second interconnect pattern formed on the other surface of the substrate and electrically connected to the first interconnect pattern;

a first plating layer formed on the first interconnect pattern surface opposite to the substrate; and

a second plating layer formed on the second interconnect pattern surface opposite to the substrate,

wherein the first and second plating layers have different properties.

According to the present invention, since the first and second plating layers are formed on the first and second interconnect patterns, oxidation of the surface of the first and second interconnect patterns can be prevented, and also the electrical contact resistance can be lowered. The first and second plating layers have different characteristics. A plating layer having appropriate adhesion properties with a resin, and a plating layer having appropriate adhesion with a conductive material commonly require different properties. The present invention provides for this by means of the first and second plating layers of different properties.

(9) A mounting substrate of the present invention comprises:

a substrate;

an interconnect pattern formed on the substrate;

a first plating layer formed on a first portion of the

interconnect pattern surface opposite to the substrate; and

a second plating layer formed on a second portion of the interconnect pattern surface opposite to the substrate,

wherein the first and second plating layers have different properties.

According to the present invention, since the first and second plating layers are formed on the interconnect pattern, oxidation of the surface of the interconnect pattern can be prevented, and also the electrical contact resistance can be lowered. The first and second plating layers have different characteristics. A plating layer having appropriate adhesion properties with a resin, and a plating layer having appropriate adhesion with a conductive material commonly require different properties. The present invention provides for this by means of the first and second plating layers of different properties.

(10) In this mounting substrate, the first plating layer may be formed to be thinner than the second plating layer.

By making the plating layer thinner, the adhesion properties with the resin are improved, and if the plating layer is made thicker, excellent bonding with the conductive material is obtained.

(11) In this mounting substrate, the first and second plating layers may be formed of different materials.

The first plating layer can be formed of a material improving the adhesion properties with a resin, and the second plating layer can be formed of a material having excellent bonding with the conductive material.

(12) On a circuit board of the present invention, the above-described semiconductor device is mounted.

(13) An electronic instrument of the present invention is equipped with the above-described semiconductor device.

(14) A method of manufacturing a mounting substrate of the present invention comprises the steps of:

immersing a substrate in a plating bath, the substrate having a plurality of through holes and an interconnect pattern formed thereon and passsing over the through holes;

electrically connecting the interconnect pattern to a cathode;

disposing a first anode to face the surface of the substrate on which the interconnect pattern is formed;

disposing a second anode to face the surface of the substrate opposite to the interconnect pattern; and

passing currents of different current densities between the first and second anodes and the cathode,

wherein a first plating layer is formed on the interconnect pattern by the current from the first anode; and

wherein a second plating layer is formed on the interconnect pattern on the side of the substrate and within the through holes by the current from the second anode.

According to the present invention, a first plating layer can be formed on one surface of the interconnect pattern by the current from the first anode, and a second plating layer can be formed on the other surface of the interconnect pattern by the current from the second anode. It should be noted that the

second plating layer is formed on the portion of the interconnect pattern exposed from the through holes.

(15) A method of manufacturing a mounting substrate of the present invention comprises the steps of:

immersing a substrate in a first plating bath, the substrate having a plurality of through holes and an interconnect pattern formed thereon and passsing over the through holes;

electrically connecting the interconnect pattern to a cathode;

forming a first plating layer on the interconnect pattern by disposing a first anode to face the surface of the substrate on which the interconnect pattern is formed and carrying out electroplating;

immersing the substrate in a second plating bath;

electrically connecting the interconnect pattern to a cathode; and

forming a second plating layer on the interconnect pattern surface looking toward the substrate in the through holes by disposing a second anode to face the surface of the substrate opposite to the interconnect pattern and carrying out electroplating.

According to the present invention, the substrate is immersed in first and second plating baths, and a first plating layer is formed on one surface of the interconnect pattern, and a second plating layer is formed on the other surface of the interconnect pattern.

(16) A method of manufacturing a mounting substrate of the present invention comprises the steps of:

forming a plurality of through holes and an interconnect pattern passing over the through holes on a substrate;

forming a first plating layer by covering the through holes with a first resist and applying electroless plating to the interconnect pattern; and

forming a second plating layer by exposing a portion of the interconnect pattern in the through holes, covering the surface of the interconnect pattern opposite to the substrate with a second resist, and applying electroless plating to the interconnect pattern in the through holes.

According to the present invention, the first and second plating layers are formed by the two operations of electroless plating.

(17) A method of manufacturing a mounting substrate of the present invention comprises the steps of:

immersing a substrate in a plating bath, wherein the substrate has a first interconnect pattern formed on one surface and a second interconnect pattern electrically connected to the first interconnect pattern and formed on the other surface;

electrically connecting the first and second interconnect patterns to a cathode;

disposing a first anode to face the first interconnect pattern;

disposing a second anode to face the second interconnect pattern; and

passing currents of different current densities between the first and second anodes and the cathode,

wherein a first plating layer is formed on the first interconnect pattern by the current from the first anode; and

wherein a second plating layer is formed on the second interconnect pattern by the current from the second anode.

According to the present invention, a first plating layer can be formed on the first interconnect pattern by the current from the first anode, and a second plating layer can be formed on the second interconnect pattern by the current from the second anode.

(18) A method of manufacturing a mounting substrate of the present invention comprises the steps of:

immersing a substrate in a first plating bath, wherein the substrate has a first interconnect pattern formed on one surface and a second interconnect pattern electrically connected to the first interconnect pattern and formed on the other surface;

electrically connecting the first interconnect pattern to a cathode;

forming a first plating layer on the first interconnect pattern, by disposing a first anode to face the first interconnect pattern and carrying out electroplating;

immersing the substrate in a second plating bath;

electrically connecting the second interconnect pattern to a cathode; and

forming a second plating layer on the second interconnect

pattern, by disposing a second anode to face the second interconnect pattern and carrying out electroplating.

According to the present invention, the substrate is immersed in first and second plating baths, a first plating layer is formed on the first interconnect pattern, and a second plating layer is formed on the second interconnect pattern.

(19) A method of manufacturing a mounting substrate of the present invention comprises the steps of:

forming a first interconnect pattern on one surface of a substrate;

forming a second interconnect pattern electrically connected to the first interconnect pattern on the other surface of the substrate;

forming a first plating layer by covering the second interconnect pattern with a first resist and applying electroless plating to the first interconnect pattern; and

forming a second plating layer by covering the first interconnect pattern with a second resist and applying electroless plating to the second interconnect pattern.

According to the present invention, the first and second plating layers are formed by the two operations of electroless plating.

(20) A method of manufacturing a mounting substrate of the present invention comprises the steps of:

forming an interconnect pattern on a substrate;

forming a first plating layer on a first portion of the interconnect pattern by covering a second portion of the

interconnect pattern with a resist and exposing the first portion, and applying electroless plating to the interconnect pattern; and

forming a second plating layer in the second portion by covering the first portion with a resist and exposing the second portion, and applying electroless plating to the interconnect pattern.

According to the present invention, the first and second plating layers are formed by the two operations of electroless plating.

(21) In this method of manufacturing a mounting substrate, the first and second plating layers may have different properties.

A plating layer having appropriate adhesion properties with a resin, and a plating layer having appropriate adhesion with a conductive material commonly require different properties. In this case, by making the current densities between the first and second anodes and the cathode different, first and second plating layers of different thicknesses may be formed. Alternatively, by making the plating fluids in the first and second plating baths different, or making the current densities between the first and second anodes and the cathode different, first and second plating layers of different thicknesses may be formed.

(22) In this method of manufacturing a mounting substrate, the first plating layer may be formed to be thinner than the second plating layer.

By making the plating layer thinner, the adhesion properties with the resin are improved, and if the plating layer is made thicker, excellent bonding with the conductive material is obtained.

(23) In this method of manufacturing a mounting substrate, the first and second plating layers may be formed of different materials.

The first plating layer can be formed of a material improving the adhesion properties with a resin, and the second plating layer can be formed of a material having excellent bonding with the conductive material.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows a semiconductor device according to a first embodiment of the present invention.

Fig. 2 shows a substrate of a semiconductor device according to the first embodiment of the present invention.

Fig. 3 shows a mounting substrate used in the first embodiment of the present invention.

Fig. 4 shows a method of manufacturing a mounting substrate according to the first embodiment of the present invention.

Fig. 5 shows a method of manufacturing a semiconductor device according to the first embodiment of the present invention.

Fig. 6 shows a method of manufacturing a mounting substrate according to a second embodiment of the present

invention.

Figs. 7A and 7B show a method of manufacturing a mounting substrate according to a third embodiment of the present invention.

Fig. 8 shows a semiconductor device according to a fourth embodiment of the present invention.

Figs. 9A and 9B show a substrate of a semiconductor device according to the fourth embodiment of the present invention.

Fig. 10 shows a semiconductor device according to a fifth embodiment of the present invention.

Figs. 11A and 11B show a method of manufacturing a mounting substrate according to the fifth embodiment of the present invention.

Fig. 12 shows a circuit board to which the present invention is applied.

Fig. 13 shows an electronic instrument equipped with a semiconductor device fabricated with application of the method of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

The present invention is now described in terms of a number of preferred embodiments, with reference to the drawings.

First Embodiment

Fig. 1 shows a first embodiment of the semiconductor device of the present invention. A semiconductor device 1

comprises a semiconductor chip 10 and a substrate 20. When the plan view form of the semiconductor chip 10 is a rectangle (a square or an oblong), along at least one side (which case includes a pair of opposing sides or all four sides), on one surface of the semiconductor chip 10 (the active surface) a plurality of electrodes 12 may be formed. Alternatively, the plurality of electrodes 12 may be arranged in the center of the semiconductor chip 10 or the vicinity thereof. On the electrodes 12 are provided bumps 14 in the form of solder balls, gold wire balls, gold plating, or the like. The electrodes 12 themselves may be in the form of bumps. Between the electrodes 12 and the bumps 14, a layer to prevent the diffusion of the bump metal, of nickel, chromium, titanium, or the like, may be applied.

There is no particular restriction on the overall form of the substrate 20, which may be a rectangle, polygon, or a combination of a plurality of rectangles, and can be a similar figure of the plan view form of the semiconductor chip 10. The thickness of the substrate 20 is commonly determined by the material used, and is not subject to particular restriction. The substrate 20 may be formed of an organic or inorganic material, or may be constituted of a combination thereof. The substrate 20 may be a flexible substrate, or may equally be a rigid substrate. The substrate 20 can be formed by punching out from a flexible substrate in the form of a tape formed of an organic resin.

Fig. 2 is a plan view of the substrate of the semiconductor device shown in Fig. 1. As shown in Figs. 1 and 2, on one surface

of the substrate 20 is formed a plurality of interconnects (leads) 22, which constitute an interconnect pattern 21. Each of the interconnects 22 has formed lands 24 and 26. The lands 24 and 26 are commonly formed to be wider than the interconnect 22. The one land 26 may be formed in a position close to the center of the substrate 20, and the other land 24 formed at an intermediate point of the interconnect 22. Of the plurality of interconnects 22, at least one or all is or are not electrically conductive to the other interconnects 22, and is or are electrically isolated. Of the plurality of interconnects 22, interconnects such as those connected in common to the power supply or ground of the semiconductor chip 10 may have the lands 24 and 26 connected together.

In the substrate 20 is formed a plurality of through holes 28. Over each of the through holes 28 passes one of the interconnects 22. The ends of the interconnects 22 may equally be positioned over the through holes 28. When a land 26 is formed at the end of an interconnect 22, the land 26 is positioned over a through hole 28.

As shown in the enlargement in Fig. 1, the interconnects 22 have formed thereon first and second plating layers 30 and 32. The interconnects 22 are formed of copper, or a two-layer construction of platinum and nickel, and the material of the plating layers 30 and 32 can be selected from nickel, palladium, nickel-gold, nickel-palladium-gold, gold, solder, and tin. The first plating layer 30 is formed on the surface of the interconnect 22 opposite to that of the substrate 20. The second

plating layer 32 is formed on the surface of the interconnect 22 facing the substrate 20 within the through hole 28. When a land 26 is positioned over the through hole 28, the second plating layer 32 is formed on the land 26. The first and second plating layers 30 and 32 have different properties as a result of differing in at least either of thickness or material.

The first plating layer 30 prevents oxidation at least over the land 24, and ensures conduction, and lowers the electrical contact resistance. Even though the first plating layer 30 is formed, intimate contact with the resin on the interconnects 22 can be obtained. For example, taking as an example of the resin an adhesive of an anisotropic conductive material, when nickel is formed as an underlayer for the plating layer 30, in order that for example a silane coupling material included in the adhesive forms a chemical compound with the nickel or with its oxide or hydroxide, the plating layer 30 is preferably formed to be thin. For example, gold plating of thickness on the order of 0.05 μm can be used for the first plating layer 30. This enables a strong bond to be obtained.

On the other hand, the second plating layer 32 is appropriate for bonding to a conductive material, such as for example external terminals. For example, gold plating of thickness on the order of 0.3 μm as the second plating layer 32 ensures good bonding with the conductive material. If the conductive material is solder, solder plating may be used for the second plating layer 32 to ensure good soldering characteristics.

The semiconductor chip 10 is mounted on the substrate 20 by face-down bonding. The bumps 14 of the semiconductor chip 10, and the interconnects 22 formed on the substrate 20 are electrically connected. Since the plating layer 30 is formed on the interconnects 22 a satisfactory electrical connection is obtained. When the lands 24 and 26 are formed on the interconnects 22, the lands 24 and bumps 14 are electrically connected. As a means of the electrical connection may be used an anisotropic conductive material 34 including conductive particles in an adhesive formed of a resin. In this case, the conductive particles are interposed between the interconnects 22 and the bumps 14 to provide electrical conduction. The anisotropic conductive material 34 may be an anisotropic conductive film or anisotropic conductive adhesive.

When the anisotropic conductive material 34 is used, it covers the surface of the interconnects 22 opposite to the surface of contact with the substrate 20, the side surfaces and the end surfaces, or in other words the surfaces not in contact with the substrate 20. When the anisotropic conductive material 34 is not used, a resin of an underfill material or the like is employed to cover the surfaces of the interconnects 22 not in contact with the substrate 20. The material covering the interconnects 22 may also cover the whole of one surface of the substrate 20. Since the first plating layer 30 formed on the interconnects 22 has appropriate adhesion properties with the resin, the resin provided on the interconnects 22 is less liable to peel off. That is to say, the anisotropic conductive material

34 is made less liable to peel off.

On the surface of the interconnects 22 facing the substrate 20, within the through holes 28 a conductive material 36 is provided. In more detail, the conductive material 36 is formed on the second plating layer 32, and projects from the through holes 28. The conductive material 36 forms external terminals. Since the second plating layer 32 has appropriate adhesion properties with the conductive material, a satisfactory electrical connection can be obtained between the conductive material 36 and the second plating layer 32. The conductive material 36 commonly consists of solder balls, but may equally be plating, or conductive projections of for example conductive resin.

Instead of the external terminals being formed by the conductive material 36, the through holes 28 may be filled with the conductive material 36, the second interconnects electrically connected to the conductive material 36 may be formed on the other surface of the substrate 20, and these second interconnects may be provided with external terminals. In this case, since the substrate 20 has interconnects formed on both surfaces it is a double-sided substrate. Furthermore, as the substrate 20 may equally be used a multi-layer substrate or a built-up substrate. When a built-up substrate or multi-layer substrate is used, if an interconnect pattern is formed on a solid ground layer which extends in plan view, then since a micro-strip construction with no surplus interconnect pattern is obtained, the signal transmission characteristics can be

improved.

The above description applies to face-down bonding using the anisotropic conductive material 34, but there is no restriction to this method of face-down bonding, and the present invention can be applied to the method of applying heat (and if necessary, pressure) to a semiconductor chip with solder bumps, the method of applying heat and pressure (and if necessary ultrasound bonding) to a semiconductor chip with gold bumps, or the face-down bonding method using the setting shrinking force of a resin. This applies also to the following embodiments.

In Fig. 1 is shown a fan-in type of semiconductor device in which the conductive material 36 forming the external terminals is provided only within the mounting region of the semiconductor chip 10, but this is not limitative of the invention. For example, the present invention can be applied to a fan-out type of semiconductor device in which external terminals are provided only outside the mounting region of the semiconductor chip 10, or a fan-in/fan-out type of semiconductor device in which this is combined with a fan-in type. In a fan-out type or fan-in/fan-out type of semiconductor device, by means of the resin provided on the interconnects 22, a stiffener may be adhered to the outside of the semiconductor chip. This applies also to the following embodiments.

Fig. 3 shows a mounting substrate of the first embodiment of the present invention. A mounting substrate 40 shown in Fig. 3 is a tape carrier, and has formed a plurality of interconnect

patterns 21 (see Fig. 1) for a plurality of semiconductor devices. Each of the interconnect patterns 21 has formed first and second plating layers 30 and 32 (see Fig. 1). The tape carrier formed by the mounting substrate 40 is punched out to obtain mounting substrates corresponding to individual semiconductor devices. A substrate having at least one interconnect pattern 21 formed is a mounting substrate, and the substrate 20 with the interconnect pattern 21 shown in Fig. 1 formed is also a mounting substrate. Alternatively, as a finished product a mounting substrate larger than the outline of the semiconductor device may be provided. In this case, before the semiconductor chip is mounted, on a part and preferably at least half of the outline position of the semiconductor device, one or preferably a plurality of holes (for example slots) can be formed, and the remainder of the outline position (for example the portions between the plurality of holes) may be punched out after mounting the semiconductor chip.

The mounting substrate 40 shown in Fig. 3 includes a substrate 42 in which is formed a plurality of through holes 28 (see Fig. 1), a plurality of interconnect patterns 21 formed on the substrate 42, first and second plating layers 30 and 32 formed on the interconnects 22 constituting the interconnect pattern 21, and at least one plating lead 44. Portions indicated by the same reference numerals as in Fig. 1 are as described above, and further description is omitted here. The construction of a typical tape carrier can be applied to the mounting substrate 40.

The plating lead 44 is formed in a position outside the punching-out position, that is, the outline position of the substrate 20 of the completed semiconductor device. Therefore, when the mounting substrate 40 is punched out, the plating lead 44 can be removed. The interconnects 22 are electrically connected to the plating lead 44. As a result, using the plating lead 44, electroplating can be carried out on the interconnects 22.

Next, Fig. 4 shows a method of manufacturing this embodiment of the mounting substrate. First, the substrate 42 which constitutes the structure of the mounting substrate 40 from which the first and second plating layers 30 and 32 have been removed is obtained. In this state, on the substrate 42, at least one or a plurality of the interconnect patterns 21 and the plating lead 44 have been formed.

A plating vat 48 is filled with a plating fluid, to provide a plating bath 46. In the plating bath 46 are disposed first and second anodes 50 and 52, and the above described substrate 42 is passed therebetween. In more detail, one surface of the substrate 42 faces the first anode 50, and the other surface faces the second anode 52. It should be noted that if the substrate 42 is a tape, a reel-to-reel process can be applied.

When the plating lead 44 formed on the substrate 42 is connected to a cathode 54 to which a potential lower than that of the anodes 50 and 52 is applied, for example, a ground potential, then currents flow between the plating lead 44 and interconnect pattern 21 (interconnects 22) connected thereto,

and each of the first and second anodes 50 and 52. In this way, electroplating is applied to the surface of the interconnect pattern 21 (interconnects 22) opposite to the substrate 42, and to the portions exposed by the through holes 28, and thus the first and second plating layers 30 and 32 can be formed.

By for example applying different voltages V1 and V2 to each of the first and second anodes 50 and 52, the current density of the current flowing from each thereof is arranged to be different. By means of this, the thicknesses of the first and second plating layers 30 and 32 can be made different.

In this way, the first and second plating layers 30 and 32 are formed on the interconnect pattern 21 (interconnects 22), and the mounting substrate 40 is obtained. It should be noted that if the substrate 42 is a tape, the mounting substrate 40 is a tape carrier.

Although not shown in the drawings, portions other than those forming electrical contacts may be covered by a permanent resist such as a solder resist, and this applies similarly to the following embodiments. In this case, plating is not applied to the portions other than those forming electrical contacts.

Next, the method of manufacturing a semiconductor device using this embodiment of the mounting substrate is described. On each of the interconnect patterns 21 formed on the above described mounting substrate 40 a semiconductor chip 10 is mounted by face-down bonding. For example, as shown in Fig. 1, the anisotropic conductive material 34 can be used. The anisotropic conductive material 34 may be provided beforehand

on the surface of the semiconductor chip 10 on which the electrodes 12 are formed, or may be provided beforehand on the surface of the mounting substrate 40 on which the interconnects 22 are formed. The anisotropic conductive material 34 may be provided to cover each individual interconnect pattern 21 separately, or the anisotropic conductive material 34 may be provided to cover a plurality of interconnect patterns 21.

As shown in Fig. 1, the conductive material 36 forming the external terminals is provided. In this way, the plurality of semiconductor chips 10 is mounted on the mounting substrate 40, and a semiconductor device assembly consisting of the result of integrating the plurality of semiconductor devices 1 is obtained.

Next, as shown in Fig. 5, the mounting substrate 40 is punched out on the outside of each semiconductor chip 10. The form in which the punching is carried out is not particularly restricted, but may be a shape similar to the plan view form of the semiconductor chip 10. For the punching out, cutting jigs 56 and 58 can be used. In this way, the semiconductor device 1 can be fabricated continuously.

Second Embodiment

Fig. 6 shows a method of manufacturing a second embodiment of the mounting substrate of the present invention. In this embodiment, the substrate 42 which constitutes the structure of the mounting substrate 40 shown in Fig. 3, from which the first and second plating layers 30 and 32 have been removed is

obtained. In this state, on the substrate 42, at least one or a plurality of the interconnect patterns 21 and the plating lead 44 have been formed.

First and second plating vats 60 and 62 are filled with a plating fluid, to provide sequentially first and second plating baths 64 and 66. In the first and second plating baths 64 and 66 are disposed first and second anodes 68 and 70. The substrate 42 is passed through the first plating bath 64 with one surface facing the first anode 68, and next is passed through the second plating bath 66 with the other surface facing the second anode 70. It should be noted that if the substrate 42 is a tape, a reel-to-reel process can be applied.

When the plating lead 44 formed on the substrate 42 is connected to a cathode 72 to which a potential lower than that of the anodes 68 and 70 is applied, for example, a ground potential, then currents flow between the plating lead 44 and interconnect pattern 21 (interconnects 22) connected thereto, and each of the first and second anodes 68 and 70. In this way, electroplating is applied to the surface of the interconnect pattern 21 (interconnects 22) opposite to the substrate 42, and to the portions exposed by the through holes 28, and thus the first and second plating layers 30 and 32 can be formed.

By for example applying different voltages V3 and V4 to each of the first and second anodes 68 and 70, the current density of the current flowing from each thereof is arranged to be different. By means of this, the thicknesses of the first and second plating layers 30 and 32 can be made different.

In this way, the first and second plating layers 30 and 32 are formed on the interconnect pattern 21 (interconnects 22), and the mounting substrate 40 shown in Fig. 3 is obtained. It should be noted that if the substrate 42 is a tape, the mounting substrate 40 is a tape carrier.

It should be noted that in this embodiment, the substrate 42 is consecutively immersed in the first and second plating baths 64 and 66, but this may equally be carried out in separate immersion processes. The first and second plating baths 64 and 66 are not restricted to containing the same metal ions, and may contain different metal ions. In that case, the material of the first and second plating layers 30 and 32 will be different. Furthermore, both the material and the thickness of the first and second plating layers 30 and 32 may be made different.

Third Embodiment

Figs. 7A and 7B show a method of manufacturing a third embodiment of the mounting substrate of the present invention. In this embodiment, the substrate 20 is obtained with the interconnect pattern 21 (interconnects 22) shown in Fig. 1 formed, but before the plating layers 30 and 32 have been formed.

First, as shown in Fig. 7A, the through holes 28 are filled with a resist 80. The resist 80 may be a resin, or it may be a removable tape or the like. By means of this, the part of the interconnects 22 exposed through the through holes 28 is covered. Then by applying electroless plating the exposed surface of the interconnects 22 is plated. The first plating layer 30 on the

surface of the interconnects 22 opposite to that of the substrate 20 is formed. The first plating layer 30 has the properties as described in the first embodiment.

Next, the resist 80 is removed, and as shown in Fig. 7B, the portions of the interconnects 22 not covered by the resist 80 are covered by a resist 82. The resist 82 may be a resin, or may be a removable tape. Above the surface of the interconnects 22 opposite to the substrate 20 is covered by the resist 82, and within the through holes 28, a part of the interconnects 22 is exposed. The first plating layer 30 is covered by the resist 82. Then when the electroless plating is carried out, the exposed surface of the interconnects 22 is plated. On the portion of the interconnects 22 exposed within the through holes 28, the second plating layer 32 is formed. The second plating layer 32 has the properties as described in the first embodiment.

By means of the above process, as shown in Fig. 1, the substrate 20 having the first and second plating layers 30 and 32 formed on the interconnects 22 is obtained, and this forms the mounting substrate. In this embodiment, the order of forming the first and second plating layers 30 and 32 is not significant. In the electroless plating step, the same material may be used for the solution and first and second plating layers 30 and 32 formed with different thicknesses, or different materials may be used for the solution and first and second plating layers 30 and 32 formed of different materials. Further, both the material and thickness of the first and second plating layers

30 and 32 may be made different.

When at least the thicknesses of the first and second plating layers 30 and 32 are being varied, a double-sided plating layer may first be formed without applying a resist, then the resist applied to the layer opposite to the layer to be made thicker, and then further plating applied only to the layer to be made thicker, after which the resist is removed.

Fourth Embodiment

Fig. 8 shows a fourth embodiment of the semiconductor device of the present invention. A semiconductor device 2 comprises a semiconductor chip 10 and a substrate 120. The semiconductor chip 10 is that described in the first embodiment, and has electrodes 12 and bumps 14. In the substrate 120 is formed a plurality of through holes 128, and in form, thickness, and substance these are the same as the substrate 20.

Fig. 9A is one plan view of the substrate of the semiconductor device shown in Fig. 8, and Fig. 9B is the other plan view. On one surface of the substrate 120 is formed a plurality of interconnects (leads) 122, constituting a first interconnect pattern 121. On each of the interconnects 122 are formed lands 124 and 126. The first interconnect pattern 121 may be the same as the interconnect pattern 21 described in the first embodiment. The land 126 shown in Fig. 9A has only to provide electrical conduction between the two sides of the substrate 120, and since no external terminals are provided, may be formed smaller than the land 26 in Fig. 1.

On the other surface of the substrate 120 is formed a plurality of interconnects (leads) 142, constituting a second interconnect pattern 141. On each of the interconnects 142 are formed lands 144 and 146. The second interconnect pattern 141 may be the same as the interconnect pattern 21 described in the first embodiment. In Fig. 9B the land 144 is formed larger, to provide for external terminals. The other land 146 has only to provide electrical conduction between the two sides of the substrate 120, and since no external terminals are provided, may be formed smaller than the land 144.

Over the plurality of through holes 128 formed on the substrate 120 pass a number of the interconnects 122 and 142 formed on each of the surfaces. The ends of the interconnects 122 and 142 may be positioned over the through holes 128. When the lands 126 and 146 are formed at the ends of the interconnects 122 and 142, the lands 126 and 146 are positioned over the through holes 128. The through holes 128 are provided with a conductive material 148, and the interconnects 122 on one surface of the substrate 120 and the interconnects 142 on the other surface are electrically connected.

It should be noted that holes communicating with the through holes 128 may be formed in a part of the interconnects 122 and 148 on both sides of the substrate 120, for example in the lands 126 and 146, and by plating or the like applied to the inner walls of these holes and the through holes 128 to provide a conductive material, the interconnects 122 and 148 on both sides of the substrate 120 may be made electrically

conductive.

As shown in enlargement in Fig. 8, on the interconnects 122 formed on one surface of the substrate 120 is formed a first plating layer 130, and on the interconnects 142 formed on the other surface of the substrate 120 is formed a second plating layer 132. The first and second plating layers 130 and 132 have different properties, by virtue of differing in at least either of thickness or material. The first plating layer 130 has the same properties as the first plating layer 30 described in the first embodiment, and the second plating layer 132 has the same properties as the second plating layer 32 described in the first embodiment. That is to say, the first plating layer 130 has good adhesion properties with resin, and the second plating layer 132 has appropriate adhesion properties with the conductive material.

The semiconductor chip 10 is mounted on the substrate 120 by face-down bonding. The bumps 14 of the semiconductor chip 10 and the interconnects 122 formed on one surface of the substrate 120 are electrically connected. Since the first plating layer 130 is formed on the interconnects 122, a satisfactory electrical connection is obtained. When the lands 124 and 126 are formed on the interconnects 122, the one set of lands 124 and the bumps 14 are electrically connected. As the means of electrical connection may be used the anisotropic conductive material 34 comprising conductive particles included in an adhesive formed of a resin. In this case, the conductive particles are interposed between the interconnects

122 and the bumps 14 and provide the electrical connection. The anisotropic conductive material 34 may be an anisotropic conductive film or an anisotropic conductive adhesive.

When the anisotropic conductive material 34 is used, portions of the interconnects 122 which are not in contact with the substrate 120 are covered by the anisotropic conductive material 34. When the anisotropic conductive material 34 is not used, the portions of the interconnects 122 which are not in contact with the substrate 120 are covered by a resin such as an underfill material. The material covering the interconnects 122 may cover the whole of one surface of the substrate 120. The first plating layer 130 formed on the interconnects 122 has good adhesion properties with resin, and therefore the resin provided over the interconnects 122 does not become detached easily.

On the interconnects 142 formed on the other side of the substrate 120 is provided a conductive material 136. In more detail, the conductive material 136 is formed on the second plating layer 132. The conductive material 136 constitutes external terminals. Since the second plating layer 132 has appropriate adhesion properties with the conductive material, a satisfactory electrical connection between the conductive material 136 and the second plating layer 132 is obtained. The conductive material 136 is commonly solder balls, but may equally comprise conductive projections such as plating, conductive resin, or the like.

At this time, other than the locations of formation of

external terminals on the second plating layer 132 side may be covered by resist. In this way, for example when forming external terminals of solder, the solder does not wet and spread to other than the locations of forming the external terminals, and at least one of the height and positional accuracy of the external terminals can be maintained by the solder.

In Fig. 8, on both sides of the substrate 120, the first and second interconnect patterns 121 and 141 are formed, and by forming the first and second plating layers 130 and 132, the mounting substrate is obtained. As a method of manufacturing this mounting substrate the method shown in Fig. 4 can be applied. That is to say, one surface of the substrate 120 faces the first anode 50, and the other surface of the substrate 120 faces the second anode 52, and the method described in the first embodiment is applied, whereby the first and second plating layers 130 and 132 of different properties can be formed.

Alternatively, as a method of manufacturing this mounting substrate, the method shown in Fig. 6 can be applied. That is to say, one surface of the substrate 120 faces the first anode 68, and the other surface of the substrate 120 faces the second anode 70, and the method described in the second embodiment is applied, whereby the first and second plating layers 130 and 132 of different properties can be formed.

Alternatively, as a method of manufacturing this mounting substrate, the method shown in Figs. 7A and 7B can be applied. That is to say, the first interconnect pattern 121 formed on one surface of the substrate 120 may be covered by a first resist

and electroless plating carried out, then this resist removed, and the second interconnect pattern 141 formed on the other surface of the substrate 120 covered by a second resist and electroless plating carried out. In this case, the method described in the third embodiment is applied.

Fifth Embodiment

Fig. 10 shows a fifth embodiment of the semiconductor device of the present invention. A semiconductor device 3 comprises a semiconductor chip 10 and a substrate 220. The semiconductor chip 10 is that described in the first embodiment, and has electrodes 12 and bumps 14. In the substrate 220 is formed a plurality of through holes 228, and in form, thickness, and substance these are the same as the substrate 20. On the substrate 220 is formed a plurality of interconnects 22 constituting an interconnect pattern 221. The interconnect pattern 221 and interconnects 222 may have the same construction as the interconnect pattern 21 and interconnects 22 described in the first embodiment. The interconnects 222 pass over the through holes 228.

In this embodiment, as shown in enlargement in Fig. 10, first and second plating layers 230 and 232 are formed on the side of the interconnect pattern 222 opposite to the substrate 220. For other parts of the construction the same construction as is shown in the first embodiment can be applied, and parts of the same construction are also indicated by the same reference numerals in Fig. 10. Although not shown in Fig. 10,

on exposed portions within the through holes 228 in the interconnects 222, to provide the conductive material 36 to form the external terminals, a plating layer having the same properties as the first plating layer 32 shown in Fig. 1 may be formed.

The first plating layer 230 has good adhesion properties with resin, and may have the same construction as the first plating layer 30 described in the first embodiment. The second plating layer 232 has appropriate adhesion properties with the conductive material, and may have the same construction as the second plating layer 32 described in the first embodiment.

The first plating layer 230 is formed in the portion (first portion) of the interconnect pattern 221 (interconnects 222) contacted by the resin, and is such as to render the resin provided thereon less liable to becoming detached. The adhesive of the anisotropic conductive material 34 is an example of the resin. The second plating layer 232 is formed in the portion (second portion) of the interconnect pattern 221 (interconnects 222) bonded to the bumps 14 as the conductive material, and provides a reliable electrical connection with the semiconductor chip 10.

On the substrate 220 shown in Fig. 10, the interconnect pattern 221 is formed, and the first and second plating layers 230 and 232 are formed, to obtain the mounting substrate.

Figs. 11A and 11B show a method of manufacturing the fifth embodiment of the mounting substrate of the present invention. In this embodiment, the substrate 220 is provided when the

interconnect pattern 221 (interconnects 222) shown in Fig. 10 has been formed, and before the first and second plating layers 230 and 232 have been formed.

First, as shown in Fig. 11A, the portion (first portion) of the interconnect pattern 221 (interconnects 222) contacted by the resin is exposed, and on the interconnect pattern 221 (interconnects 222) a resist 240 is formed. The resist 240 is formed to exclude the portion (second portion) bonding with the conductive material. It should be noted that within the through holes 228 may also be filled with the resist 240. The resist 240 may be a resin, or may be a removable tape. Then when electroless plating is carried out, the exposed surface of the interconnects 222 is plated. For example, the first plating layer 230 is formed on the surface of the interconnects 222 opposite to the substrate 20, in the portion (first portion) contacted by the resin.

Next, the resist 240 is removed, and as shown in Fig. 11B, the portion (first portion) of the interconnects 222 contacted by the resin is covered with a resist 242. The resist 242 may be a resin, or may be a removable tape. Within the through holes 228, a part of the interconnects 222 may be exposed. The first plating layer 230 is covered by the resist 242. When electroless plating is carried out, the exposed surface of the interconnects 222 is plated. On the portion (second portion) of the interconnects 222 bonding with the bumps 14 the second plating layer 232 is formed. The same plating layer may be formed on the exposed portion of the interconnects 222 within the through

holes 228.

Plating can be carried out on the whole surface of the interconnect pattern 221, and after the portions other than those required, for example other than the second portion and within the through holes 228 have been covered with a resist, if further plating is carried out, plating of the necessary thickness and type can be applied to the necessary portions only.

By means of the above process, the first and second plating layers 230 and 232 are formed on the interconnects 222, and the substrate 220 is obtained, and this constitutes the mounting substrate. In this embodiment, the order of forming the first and second plating layers 230 and 232 is not significant. In the electroless plating step of forming the first and second plating layers 230 and 232, there is no restriction to the use of the same material for the solution, and different materials may be used for the solution. In this case the first and second plating layers 230 and 232 are formed of different materials. Further, both the material and thickness of the first and second plating layers 230 and 232 may be made different.

In Fig. 12 is shown a circuit board 1000 on which is mounted this embodiment of the semiconductor device 1. For the circuit board 1000 is generally used an organic substrate such as a glass epoxy substrate or the like. On the circuit board 1000, an interconnect pattern 1100 of for example copper is formed to constitute a desired circuit, then by mechanical connection of

this interconnect pattern and the external terminals 36 of the semiconductor device 1, electrical connection is achieved.

Then as an electronic instrument 1200 equipped with the semiconductor device 1 to which the present invention is applied, in Fig. 13 is shown a notebook personal computer 1100.

It should be noted that the above-described "semiconductor element" that is structural component of the present invention may be replaced by "electronic element," and an electronic element (either an active element or a passive element) can be mounted on a substrate to fabricate an electronic component, in the same way as a semiconductor chip. As electronic components manufactured by using such an electronic element may be cited, for example, resistors, capacitors, coils, oscillators, filters, temperature sensors, thermistors, varistors, variable resistors, and fuses.

CLAIMS

1. A semiconductor device comprising:

a substrate in which a plurality of through holes are formed;

an interconnect pattern formed on the substrate and passing over the through holes;

a first plating layer formed on the interconnect pattern surface opposite to the substrate;

a second plating layer formed on the interconnect pattern surface looking toward the substrate in the through holes;

a semiconductor chip mounted on the substrate and electrically connected to the first plating layer;

a resin provided on the first plating layer; and

a conductive material provided on the second plating layer,

wherein the first and second plating layers have different properties.

2. A semiconductor device comprising:

a substrate;

a first interconnect pattern formed on one surface of the substrate;

a second interconnect pattern formed on the other surface of the substrate and electrically connected to the first interconnect pattern;

a first plating layer formed on the first interconnect

pattern surface opposite to the substrate;

a second plating layer formed on the second interconnect pattern surface opposite to the substrate;

a semiconductor chip mounted on the substrate and electrically connected to the first plating layer;

a resin provided on the first plating layer; and

a conductive material provided on the second plating layer,

wherein the first and second plating layers have different properties.

3. A semiconductor device comprising:

a substrate;

an interconnect pattern formed on the substrate;

a first plating layer formed on a first portion of the interconnect pattern surface opposite to the substrate;

a second plating layer formed on a second portion of the interconnect pattern surface opposite to the substrate;

a resin provided on the first plating layer;

a conductive material provided on the second plating layer; and

a semiconductor chip mounted on the substrate and electrically connected to the conductive material,

wherein the first and second plating layers have different properties.

4. The semiconductor device as defined in claim 1,

wherein the first plating layer is formed to be thinner than the second plating layer.

5. The semiconductor device as defined in claim 2, wherein the first plating layer is formed to be thinner than the second plating layer.

6. The semiconductor device as defined in claim 3, wherein the first plating layer is formed to be thinner than the second plating layer.

7. The semiconductor device as defined in claim 1, wherein the first and second plating layers are formed of different materials.

8. The semiconductor device as defined in claim 2, wherein the first and second plating layers are formed of different materials.

9. The semiconductor device as defined in claim 3, wherein the first and second plating layers are formed of different materials.

10. The semiconductor device as defined in claim 1, wherein the resin is an adhesive, and includes conductive particles to constitute an anisotropic conductive material; and wherein the semiconductor chip is mounted by face-down

bonding with the anisotropic conductive material interposed.

11. The semiconductor device as defined in claim 2,

wherein the resin is an adhesive, and includes conductive particles, to constitute an anisotropic conductive material; and

wherein the semiconductor chip is mounted by face-down bonding with the anisotropic conductive material interposed.

12. The semiconductor device as defined in claim 3,

wherein the resin is an adhesive, and includes conductive particles, to constitute an anisotropic conductive material; and

wherein the semiconductor chip is mounted by face-down bonding with the anisotropic conductive material interposed.

13. A mounting substrate comprising:

a substrate in which a plurality of through holes are formed;

an interconnect pattern formed on the substrate and passing over the through holes;

a first plating layer formed on the interconnect pattern surface opposite to the substrate; and

a second plating layer formed on the interconnect pattern surface looking toward the substrate in the through holes,

wherein the first and second plating layers have different properties.

14. A mounting substrate comprising:

a substrate;

a first interconnect pattern formed on one surface of the substrate;

a second interconnect pattern formed on the other surface of the substrate and electrically connected to the first interconnect pattern;

a first plating layer formed on the first interconnect pattern surface opposite to the substrate; and

a second plating layer formed on the second interconnect pattern surface opposite to the substrate,

wherein the first and second plating layers have different properties.

15. A mounting substrate comprising:

a substrate;

an interconnect pattern formed on the substrate;

a first plating layer formed on a first portion of the interconnect pattern surface opposite to the substrate; and

a second plating layer formed on a second portion of the interconnect pattern surface opposite to the substrate,

wherein the first and second plating layers have different properties.

16. The mounting substrate as defined in claim 13, wherein the first plating layer is formed to be thinner

than the second plating layer.

17. The mounting substrate as defined in claim 14, wherein the first plating layer is formed to be thinner than the second plating layer.

18. The mounting substrate as defined in claim 15, wherein the first plating layer is formed to be thinner than the second plating layer.

19. The mounting substrate as defined in claim 13, wherein the first and second plating layers are formed of different materials.

20. The mounting substrate as defined in claim 14, wherein the first and second plating layers are formed of different materials.

21. The mounting substrate as defined in claim 15, wherein the first and second plating layers are formed of different materials.

22. A circuit board on which is mounted the semiconductor device as defined in any of claims 1, 4, 7, and 10.

23. A circuit board on which is mounted the semiconductor device as defined in any of claims 2, 5, 8, and 11.

24. A circuit board on which is mounted the semiconductor device as defined in any of claims 3, 6, 9, and 12.

25. An electronic instrument equipped with the semiconductor device as defined in any of claims 1, 4, 7, and 10.

26. An electronic instrument equipped with the semiconductor device as defined in any of claims 2, 5, 8, and 11.

27. An electronic instrument equipped with the semiconductor device as defined in any of claims 3, 6, 9, and 12.

28. A method of manufacturing a mounting substrate, comprising the steps of:

immersing a substrate in a plating bath, the substrate having a plurality of through holes and an interconnect pattern formed thereon and passsing over the through holes;

electrically connecting the interconnect pattern to a cathode;

disposing a first anode to face the surface of the substrate on which the interconnect pattern is formed;

disposing a second anode to face the surface of the substrate opposite to the interconnect pattern; and

passing currents of different current densities between the first and second anodes and the cathode,

wherein a first plating layer is formed on the

interconnect pattern by the current from the first anode; and

wherein a second plating layer is formed on the interconnect pattern on the side of the substrate and within the through holes by the current from the second anode.

29. A method of manufacturing a mounting substrate, comprising the steps of:

immersing a substrate in a first plating bath, the substrate having a plurality of through holes and an interconnect pattern formed thereon and passing over the through holes;

electrically connecting the interconnect pattern to a cathode;

forming a first plating layer on the interconnect pattern by disposing a first anode to face the surface of the substrate on which the interconnect pattern is formed and carrying out electroplating;

immersing the substrate in a second plating bath;

electrically connecting the interconnect pattern to a cathode; and

forming a second plating layer on the interconnect pattern surface looking toward the substrate in the through holes by disposing a second anode to face the surface of the substrate opposite to the interconnect pattern and carrying out electroplating.

30. A method of manufacturing a mounting substrate,

comprising the steps of:

forming a plurality of through holes and an interconnect pattern passing over the through holes on a substrate;

forming a first plating layer by covering the through holes with a first resist and applying electroless plating to the interconnect pattern; and

forming a second plating layer by exposing a portion of the interconnect pattern in the through holes, covering the surface of the interconnect pattern opposite to the substrate with a second resist, and applying electroless plating to the interconnect pattern in the through holes.

31. A method of manufacturing a mounting substrate, comprising the steps of:

immersing a substrate in a plating bath, wherein the substrate has a first interconnect pattern formed on one surface and a second interconnect pattern electrically connected to the first interconnect pattern and formed on the other surface;

electrically connecting the first and second interconnect patterns to a cathode;

disposing a first anode to face the first interconnect pattern;

disposing a second anode to face the second interconnect pattern; and

passing currents of different current densities between the first and second anodes and the cathode,

wherein a first plating layer is formed on the first

interconnect pattern by the current from the first anode; and

wherein a second plating layer is formed on the second interconnect pattern by the current from the second anode.

32. A method of manufacturing a mounting substrate, comprising the steps of:

immersing a substrate in a first plating bath, wherein the substrate has a first interconnect pattern formed on one surface and a second interconnect pattern electrically connected to the first interconnect pattern and formed on the other surface;

electrically connecting the first interconnect pattern to a cathode;

forming a first plating layer on the first interconnect pattern, by disposing a first anode to face the first interconnect pattern and carrying out electroplating;

immersing the substrate in a second plating bath;

electrically connecting the second interconnect pattern to a cathode; and

forming a second plating layer on the second interconnect pattern, by disposing a second anode to face the second interconnect pattern and carrying out electroplating.

33. A method of manufacturing a mounting substrate, comprising the steps of:

forming a first interconnect pattern on one surface of a substrate;

forming a second interconnect pattern electrically connected to the first interconnect pattern on the other surface of the substrate;

forming a first plating layer by covering the second interconnect pattern with a first resist and applying electroless plating to the first interconnect pattern; and

forming a second plating layer by covering the first interconnect pattern with a second resist and applying electroless plating to the second interconnect pattern.

34. A method of manufacturing a mounting substrate, comprising the steps of:

forming an interconnect pattern on a substrate;

forming a first plating layer on a first portion of the interconnect pattern by covering a second portion of the interconnect pattern with a resist and exposing the first portion, and applying electroless plating to the interconnect pattern; and

forming a second plating layer in the second portion by covering the first portion with a resist and exposing the second portion, and applying electroless plating to the interconnect pattern.

35. The method of manufacturing a mounting substrate as defined in claim 28,

wherein the first and second plating layers have different properties.

36. The method of manufacturing a mounting substrate as defined in of claim 29,

wherein the first and second plating layers have different properties.

37. The method of manufacturing a mounting substrate as defined in claim 30,

wherein the first and second plating layers have different properties.

38. The method of manufacturing a mounting substrate as defined in claim 31,

wherein the first and second plating layers have different properties.

39. The method of manufacturing a mounting substrate as defined in claim 32,

wherein the first and second plating layers have different properties.

40. The method of manufacturing a mounting substrate as defined in claim 33,

wherein the first and second plating layers have different properties.

41. The method of manufacturing a mounting substrate as

defined in claim 34,

wherein the first and second plating layers have different properties.

42. The method of manufacturing a mounting substrate as defined in claim 28,

wherein the first plating layer is formed to be thinner than the second plating layer.

43. The method of manufacturing a mounting substrate as defined in claim 29,

wherein the first plating layer is formed to be thinner than the second plating layer.

44. The method of manufacturing a mounting substrate as defined in claim 30,

wherein the first plating layer is formed to be thinner than the second plating layer.

45. The method of manufacturing a mounting substrate as defined in claim 31,

wherein the first plating layer is formed to be thinner than the second plating layer.

46. The method of manufacturing a mounting substrate as defined in claim 32,

wherein the first plating layer is formed to be thinner

than the second plating layer.

47. The method of manufacturing a mounting substrate as defined in claim 33,

wherein the first plating layer is formed to be thinner than the second plating layer.

48. The method of manufacturing a mounting substrate as defined in claim 34,

wherein the first plating layer is formed to be thinner than the second plating layer.

49. The method of manufacturing a mounting substrate as defined in claim 29,

wherein the first and second plating layers are formed of different materials.

50. The method of manufacturing a mounting substrate as defined in claim 30,

wherein the first and second plating layers are formed of different materials.

51. The method of manufacturing a mounting substrate as defined in claim 32,

wherein the first and second plating layers are formed of different materials.

52. The method of manufacturing a mounting substrate as defined in claim 33,

wherein the first and second plating layers are formed of different materials.

53. The method of manufacturing a mounting substrate as defined in claim 34,

wherein the first and second plating layers are formed of different materials.

ABSTRACT

There is provided a semiconductor device comprising: a first plating layer (30) formed on one surface of an interconnect pattern (21); a second plating layer (32) formed within through holes (28) in the interconnect pattern (21); a semiconductor chip (10) electrically connected to the first plating layer (30); an anisotropic conductive material (34) provided on the first plating layer (30); and a conductive material (36) provided on the second plating layer (32), wherein the first plating layer (30) has appropriate adhesion properties with the anisotropic conductive material (34), and the second plating layer (32) has appropriate adhesion properties with the conductive material (36).

FIG. 1

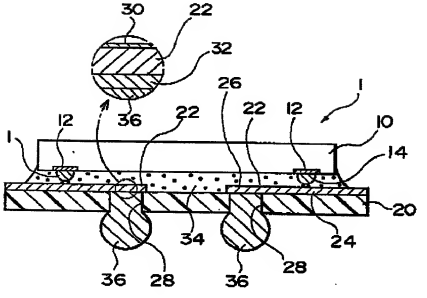
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FIG. 2

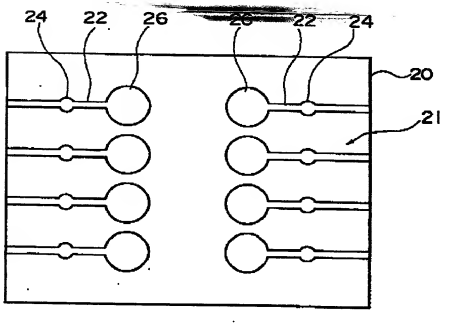
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FIG. 3

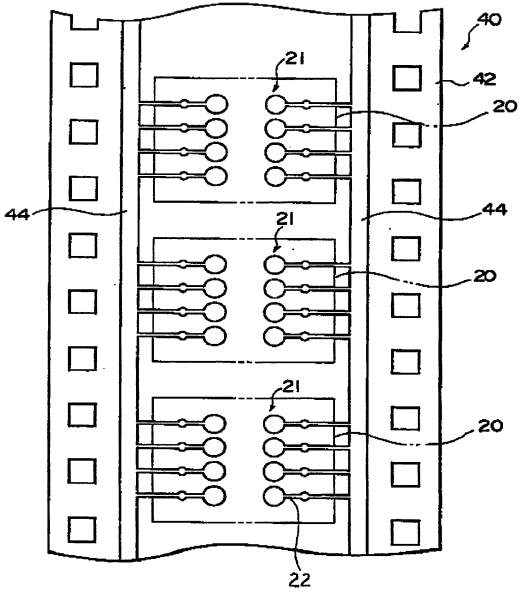


FIG. 4

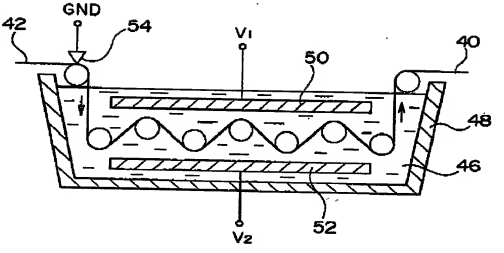
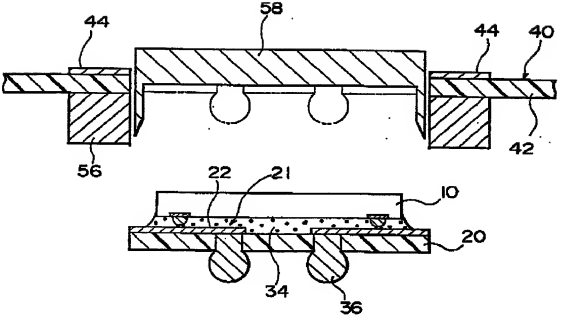


FIG. 5



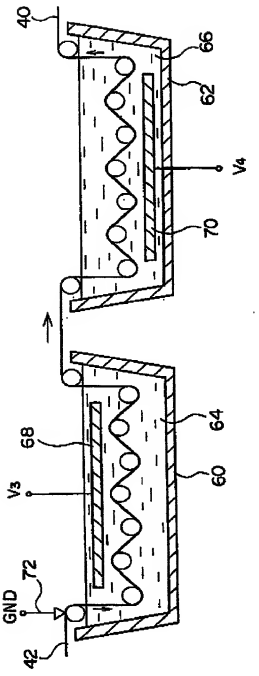


FIG. 6

FIG. 7A

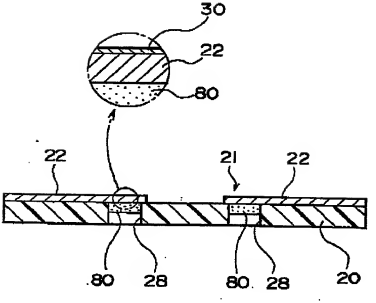


FIG. 7B

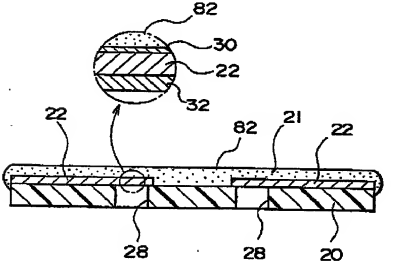


FIG. 8

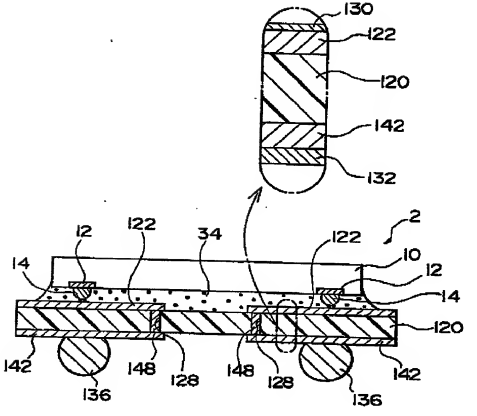

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FIG. 9A

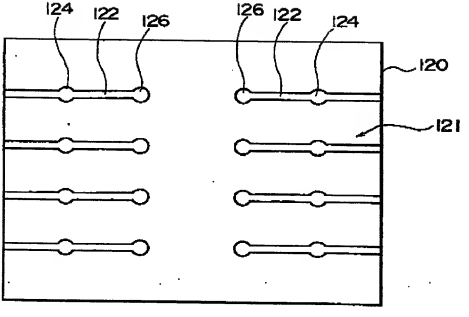


FIG. 9B

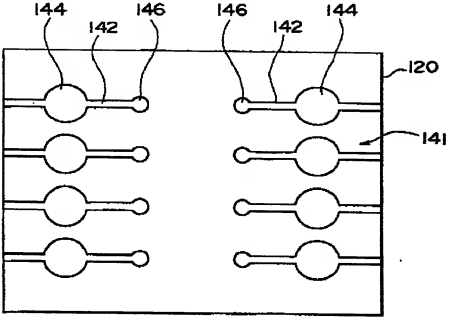


FIG. 10

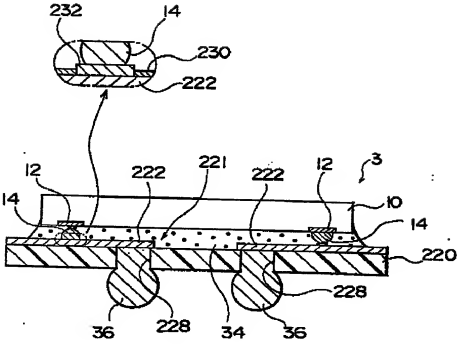


FIG. 11A

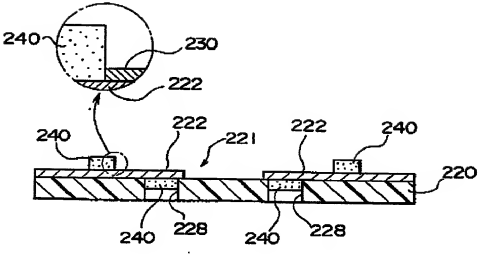


FIG. 11B

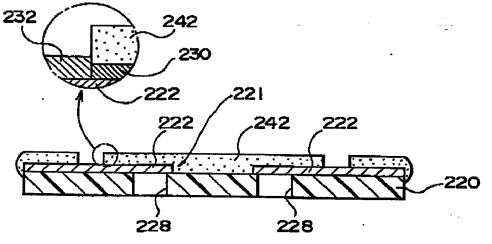


FIG. 12

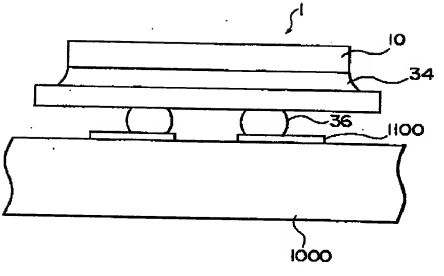
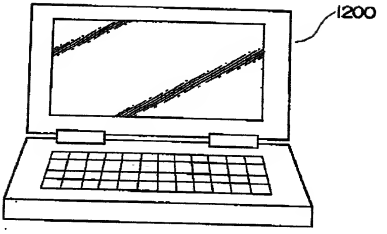


FIG. 13



Seiko Epson Ref. No.: F004947US00 | Attorney's Ref. No.: 107281

Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は、下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

半導体装置、実装基板及びその製造方法、回路基板並びに電子機器

SEMICONDCUTOR DEVICE, MOUNTING SUBSTRATE AND METHOD OF MANUFACTURING MOUNTING SUBSTRATE, CIRCUIT BOARD, AND ELECTRONIC INSTRUMENT

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

the specification of which is attached hereto unless the following box is checked:

☐ _____に提出され、米国出願番号または特許協定条約 国際出願番号を _____ とし、（該当する場合） _____ に訂正されました。

☐ was filed on _____ as United States Application Number or PCT International Application Number _____ and was amended on _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

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I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

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I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Not Claimed 優先権主張なし
11-039623(P)	JAPAN	18/February/1999	☐
			☐

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Application No.) (出願番号)	(Filing Date) (出願日)

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(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)
PCT/JP00/00894	17/February/2000	Pending

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

PTO/SB/106 (8-96)
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William P. Berridge, (Reg. 30,024)
Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)
Caroline D. Dennison, (Reg.34,494)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

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Kirk M. Hudson, (Reg. 27,562)
Thomas J. Pardini, (Reg. 30,411)
Edward P. Walker, (Reg. 31,450)
Robert A. Miller, (Reg. 32,771)
Mario A. Costantino, (Reg. 33,565)
Caroline D. Dennison, (Reg.34,494)

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国籍 日本	Citizenship Japan
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第二共同発明者の署名 日付	Second inventor's signature Date
住所 日本国、＿＿＿＿ ＿＿＿＿	Residence ＿＿＿＿ ＿＿＿＿ Japan
国籍	Citizenship
私書箱	Post Office Address

(第三以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for third and subsequent joint inventors.)